REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 1 so as to clearly define the subject matter of the present invention. More specifically, claim 1 has been amended to include the limitations of original claim 5, which has been cancelled. In addition, claim 1 has been amended to recite that the substrate temperature during the formation of the p-type nitride semiconductor layer is 950°C or higher. Support for the amendment can be found, for example, on page 9, lines 19-28 of the specification. In addition, new claims 13-14 have been added. Support for new claim 13 can be found, for example, on page 2, lines 6-10, and support for new claim 14 can be found, for example, in Fig. 2 and the corresponding disclosure in the specification.

For the following reasons, Applicants respectfully submit that the pending claims are patentable over the cited prior art reference.

II. The Rejection Of Claims 1-10 Under 35 U.S.C. § 102

Claims 1-10 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,117,700 to Orita. For the following reasons, Applicants respectfully submit that the pending claims are patentable over Orita.

As recited by claim 1, the present invention relates to a method for forming a p-

type GaN semiconductor layer with low resistance, which comprises the steps of: (1) forming a p-type GaN semiconductor layer on a substrate which is heated to a temperature of 950°C or higher, (2) cooling the substrate to a temperature of approximately 600°C, and (3) maintaining the atmosphere during the cooling process such that it contains 0%-50% hydrogen.

Accordingly, the present invention provides a cooling process after forming the GaN semiconductor layer, during which the substrate temperature is brought down to approximately 600°C and the atmosphere comprises 0%-50% hydrogen. As detailed in the specification, the foregoing method results in the formation of a low resistance p-type GaN semiconductor layer.

Turning to the cited prior art, while also directed to the formation of a low resistance p-type GaN layer, at a minimum, Orita does not disclose or suggest the claimed cooling process of the present invention, in which the hydrogen content of the atmosphere is maintained in the range of 0%-50% while the substrate is reduced to a temperature of approximately 600°C. In contrast to the claimed invention, Orita teaches performing a plasma treatment and a subsequent annealing process to obtain the low resistance p-type GaN layer. Specifically, as set forth in col. 6, lines 6-13 of Orita, after formation of the first and second Mg-doped layers 16A and 17A, the epitaxial substrate is introduced into a plasma processor so as to form p-type cladding layer 16B and p-type contact layer 17B having low resistivity. Thereafter, the substrate

of Orita is etched and annealed. Again, nowhere does Orita disclose or suggest the claimed cooling process of the present invention, during which the hydrogen content of the atmosphere is maintained within the limits set forth in claim 1 as the temperature of the substrate is reduced to approximately 600°C.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and at a minimum, Orita fails to disclose the claimed cooling process of the present invention, it is clear that Orita does not anticipate amended claim 1, or any claim dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that claims 2-4 and 6-14 are also in condition for allowance.

Furthermore, with regard to claim 4, the claim recites that during the semiconductor layer forming process, the atmosphere is maintained such that it

contains 5%-70% hydrogen. The present invention utilizes hydrogen not only as a carrier gas, but also as a controlling agent to inactivate the p-type dopant. While Orita suggests hydrogen may be utilized as a carrier gas, Orita is silent as to the percentage of hydrogen in the atmosphere. As the claimed percentages are clearly not inherent in Orita, it is clear that Orita also fails to disclose or suggest the subject matter of claim 4.

In addition, new claim 13 recites that the cooling process causes the substrate temperature to be reduced from the growth temperature to approximately 600°C within 5 minutes. As Orita does not disclose a cooling process, it is also clear that Orita does not disclose or suggest new claim 13.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an

Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 4/16/02

By: _____
Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000
Facsimile: 202-756-8087

WDC99 582606-1.043890.0449

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claim 5, without prejudice.

Please amend claim 1 and add new claims13 and 14 as follows:

1. (Amended) A method for manufacturing p-type nitride semiconductor comprising:

a semiconductor layer forming process for forming a low resistivity p-type nitride semiconductor layer on a substrate held at a temperature of [600°C] 950°C or higher by introducing p-type dopant source, nitrogen source and Group III source on said substrate; and

a cooling process for cooling the substrate bearing said p-type nitride semiconductor layer[;],

wherein during said cooling process, the substrate is in an atmosphere containing 0% - 50% hydrogen, and the temperature of the substrate is reduced to approximately 600°C, and

wherein [The] the hole carrier concentration of said p-type nitride semiconductor layer decreases during said cooling process.

--13. (New) The method for manufacturing p-type nitride semiconductor recited in claim 1 or claim 2,

wherein said cooling process cools the substrate from the substrate temperature in said semiconductor layer forming process to 600°C within 5 min.

14. (New) The method of manufacturing the p-type nitride semiconductor recited in claim 1, wherein the hydrogen content of said atmosphere is greater than 0%. --